FLEXIBLE INTERRUPT CONTROLLER THAT INCLUDES AN INTERRUPT FORCE REGISTER

Abstract of the Invention

A flexible interrupt controller (28) that includes an interrupt force register (120) is presented. Hardware interrupts (102) that are presently asserted by their respective hardware sources are stored in an interrupt source register (110) included in the interrupt controller (28). An independent interrupt force register (120) stores currently pending software interrupts (104) which may be asserted through the execution of software routines by the central processing unit (CPU) (12) within the data processing system (10). In one embodiment, each bit location in the interrupt source register (110) has a corresponding bit location in the interrupt force register (120), and each bit in the interrupt force register (120) is logically OR-ed with the corresponding bit in the interrupt source register (110). Results of the logical OR operation are stored in an interrupt pending register (160) and the contents of the interrupt pending register (160) is bit wise OR-ed together in order to generate an interrupt request signal (174) provided to the CPU (12).